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EXAMINER	
VLAHOS, SOPHIA	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/555,096	KAJIWARA, YOSHIYUKI	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9 and 10* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments received on 6/02/2009 with respect to the rejection of claims 1, 4, 5, 9 under 35 U.S.C 103(a) have been considered but are moot in view of the new ground(s) of rejection.

Specification

2. The objection to the specification for incorporating by reference a foreign application or patent (not published in the English language) is withdrawn in view of the translation of the Foreign Priority Documents submitted by Applicant (6/02/2009).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vis (U.S. 7,012,772) in view of Fermo et al. “Simplified Volterra Filters for Acoustic Echo Cancellation in GSM receivers”, September 2000 and N.B. Jones et al. “Digital Signal Processing”, IEE Control Engineering Series 42, 1990, page 86 (source http://books.google.com/).

With respect to claim 1, Vis discloses: a second-order Volterra filter configured to equalize an input signal (Fig. 3, block 18 is the quadratic (or second order) order equalizing function block of a second-order Volterra filter, column 4, lines 54-64) , wherein a quadratic section of said second-order Volterra filter configured to implement a quadratic term of said second-order Volterra filter (column 4, lines 54-57).

Vis does not expressly disclose: the quadratic section of said second-order Volterra filter configured to implement a quadratic term of said second-order Volterra filter includes a multiplication unit configured to multiply a first input signal with a second input signal to produce a product signal; said multiplication unit including, one or more delay units connected in series with one another and configured to delay a signal output form said multiplication unit, each by a unit time, a multiplier configured to multiply a signal output from said multiplication unit and a signal output from each of said one or more delay units, each with a preset coefficient, said multiplier being further configured to update each preset coefficient every unit time, an adder configured to sum outputs of said multiplier together.

In the same field of endeavor, (systems using Volterra filters), Fermo et al. disclose: a quadratic section of a second-order Volterra filter configured to implement a quadratic term of said second-order Volterra filter includes a multiplication unit configured to multiply a first input signal and a second input signal together (page 2, Fig. 3, simplified second order (quadratic) Volterra filter, the multiplication unit comprises the top row of components to the left of adder which outputs signal y(n), i.e. the multiplication unit comprises a mixer and an FIR filter in each row, see also left column

on same page for more details, and the product signal is the signal supplied to each of FIR filters).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Vis based on Fermo et al so that a simplified Volterra filter which approximates a second order filter is used, resulting in high computational resource savings (Fermo, page 2, first paragraph on left column).

Notice that Fermo et al. only discloses FIR filters receiving the output of the multipliers of the Volterra filter, and not: said multiplication unit including one or more delay units connected in series with one another and configured to delay a signal output from said multiplication unit, each by a time unit , a multiplier configured to multiply a signal output from said multiplication unit and a signal output from each of said delaying means, each with a preset coefficient, said multiplier being further configured to update each preset coefficient every unit time, and an adder configured to sum outputs of said multiplier together.

In the field of digital filter design, Jones et al. discloses: a multiplication unit (an FIR filter) including : one or more series-connected delaying units and configured to delay an input signal, each by a unit time(page 86, Fig. 7.5 each of the “z-1” blocks is a delay unit); a multiplier configured to multiply an input signal and a signal output from each of said one or more delay units, each with a preset coefficient (multiplication of the input signal xk by ao and multiplication of the delayed signal xk-1 by a1, to implement equation 7.9), and an adder configured to sum outputs of said multiplier together (Fig. 7.5 summing block).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Vis and Fermo based on Jones et al. so that stable FIR filters (page 86 of Jones et al.) are used to implement the quadratic section of the second order Volterra filter of Vis.

(Incorporating the teachings of Fermo and Jones in the system of Vis is seen to disclose all of the limitations of claim 1, including the updating of the FIR coefficients of the quadratic section of the Volterra filter, based on an LMS update algorithm as taught by Vis, Fig. 3, block 20 updates coefficients used by the non-linear (quadratic) portion of the Volterra filter and the multiplier (part of the FIR filter) functions on a signal out of the mixer (as shown in Fig. 3 of Volterra, and delayed versions of it)).

With respect to claim 2, the system obtained by modifying Vis based on Fermo and Jones further includes: wherein said quadratic section includes a plurality of multiplication units, one of said multiplication units being configured to employ a signal not delayed from said first input signal, as said second signal, the remaining ones of said plurality of multiplication units each being configured to employ a signal delayed a preset time from said first input signal, as said second input signal (Fig. 3 of Fermo shows a plurality of multiplication units, the first one including the first (top) branch mixer and FIR filter, employs first signal x(n) and multiplies it with a second signal (the undelayed signal shown in Fig. 3 supplied to mixer from the "top"); and each of the remaining multiplication units multiply the first signal x(n) with a delayed version (z^{-1}, 2^{z-1}, and so on) of the first signal).

With respect to claim 3, the system obtained by modifying Vis based on Fermo and Jones further includes: wherein said quadratic section includes n of said multiplication units (Fig. 3 of Fermo, for example n=4), n being an integer not less than 1, a kth one of said plurality of multiplication units, k being an integer such that $1 \leq k \leq n$ being configured to employ signal corresponding to said first input signal delayed by k-1 times of said unit time as said second input signal (Fig. 3 of Fermo where n=4, and as an example k=3 (corresponding to the third (row) multiplication unit), which multiplies the first signal with a second signal (which is the first signal delayed by 3-1=2 delay times)).

Method claim 4 is rejected based on a rationale similar to the one used to reject apparatus claim 1 above

With respect to claim 5, Vis discloses: a linear section of the second-order Volterra filter, the linear section being configured to implement a linear term of said second-order Volterra filter and to linearly equalize said input signal (Fig. 3, block 12 implements the linear term of a second order Volterra filter, column 4, lines 54-64); a quadratic section of the second-order Volterra filter, the quadratic section being configured to implement a quadratic term of said second-order Volterra filter to non-linearly equalize said input signal (Fig. 3, block 18 is the second order equalizing function block of the Volterra filter); a first adder configured to sum a signal output from

said linear section and a signal output from said quadratic section together (Fig. 3, adder 34, column 4, lines 60-64); a processor configured to execute most likelihood decoding for a signal output from said first adder (Fig. 3, combination of blocks 28, 30, 20, column 5, lines 6-21, the shown circuitry comprise a processor), the processor being further configured to detect an error, at a preset unit time, between a signal output from said first adder and a target signal (column 5, lines 6-25, signal 22 ek is the squared error signal which the LMS attempts to minimize)

Vis does not expressly disclose: wherein said quadratic section includes a multiplication unit configured to multiply a first input signal and a second input signal together; said multiplication unit including one or more series-connected delaying units configured to delay signals output from said multiplication unit each by the preset unit time, a multiplier configured to multiply a signal output from said multiplication unit and a signal output from each of said delaying units, each with a preset coefficient, said multiplier being further configured to update each preset coefficient every preset unit time based on an error detected by said processor, and a second adder configured to sum outputs of said multiplier together.

In the same field of endeavor, (systems using Volterra filters), Fermo et al. disclose: a quadratic section of a second-order Volterra filter, the quadratic section being configured to implement a quadratic term of said second-order Volterra filter wherein said quadratic section includes a multiplication unit configured to multiply a first input signal and a second input signal together (page 2, Fig. 3, simplified second order (quadratic) Volterra filter, the multiplication means comprises the top row of components

to the left of adder which outputs signal y(n), i.e. the multiplication unit comprises a mixer and an FIR filter in each row, see also left column on same page for more details, and the product signal is the signal supplied to each of FIR filters).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Vis based on Fermo et al so that a simplified Volterra filter which approximates a second order filter is used, resulting in high computational resource savings (Fermo, page 2, first paragraph on left column).

Notice that Fermo et al. only discloses FIR filters receiving the output of the multipliers of the Volterra filter, and not: said multiplication unit including one or more series-connected delaying units configured to delay signals output from said multiplication unit each by a preset unit time, at multiplier configured to multiply a signal output from said multiplication unit and a signal output from each of said one or more series-connected delaying units each with a preset coefficient, said multiplier being further configured to update each preset coefficient every preset unit time based on an error detected by said processor, and a second adder configured to sum outputs of said multiplier together.

In the field of digital filter design, Jones et al. discloses: a multiplication unit (an FIR filter) including : one or more series-connected delaying units configured to delay input signals each by a preset unit time (page 86, Fig. 7.5 each of the “z-1” blocks is a delay unit); a multiplier configured to multiply an input signal and a signal output from each of said one or more series connected delaying units (multiplication of the input signal xk by ao and multiplication of the delayed signal xk-1 by a1, to implement

equation 7.9), each with a preset coefficient, and a adder configured to sum outputs of said multiplier together (Fig. 7.5 summing block).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Vis and Fermo based on Jones et al. so that stable FIR filters (page 86 of Jones et al.) are used to implement the quadratic section of the second order Volterra filter of Vis.

(Incorporating the teachings of Fermo and Jones in the system of Vis is seen to disclose all of the limitations of claim 5, including the updating of the FIR coefficients of the quadratic section of the Volterra filter, based on an error detected by said processor (see the LMS update algorithm) as taught by Vis, Fig. 3, block 20 updates coefficients used by the non-linear (quadratic) portion of the Volterra filter and the multiplier (part of the FIR filter) functions on a signal out of the mixer (as shown in Fig. 3 of Volterra, and delayed versions of it) and the adder which is part of the digital FIR filter is a second adder in the system of Vis et al. considering that adder 34 is the first adder).

With respect to claims 6-7, claims 6-7 are rejected based on a rationale similar to the one used to reject claim 2-3 above.

With respect to claim 9 method claim 9 is rejected based on a rationale similar to the one used to reject apparatus claim 5 above.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vis (U.S. 7,012,772) in view of Fermo et al. "Simplified Volterra Filters for Acoustic Echo Cancellation in GSM receivers", September 2000 and N.B. Jones et al. "Digital Signal Processing", IEE Control Engineering Series 42, 1990, page 86 (source http://books.google.com/), as applied to claim 1 and further in view of McIntyre et al. (U.S. 5,422,805).

With respect to claim 10, neither Vis nor Fermo or Jones expressly disclose: wherein said multiplication unit further includes a shifter configured to left-shift the product signal to produce the signal output form said multiplication unit.

In the field of number multiplication, McIntyre et al. discloses: a multiplication unit which includes a shifter configured to left-shift the product signal to produce the signal output form said multiplication unit (Fig. 3, block 33, column 9, lines 9-13).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Vis et al. based on McIntyre to scale the product to meet specific requirements in the circuits.

Allowable Subject Matter

6. Claims 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is (571)272-5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SOPHIA VLAHOS/
Examiner, Art Unit 2611
7/21/2009

/Mohammad H Ghayour/

Supervisory Patent Examiner, Art Unit 2611